Complementary 20-V (D-S) MOSFET

CHARACTERISTICS

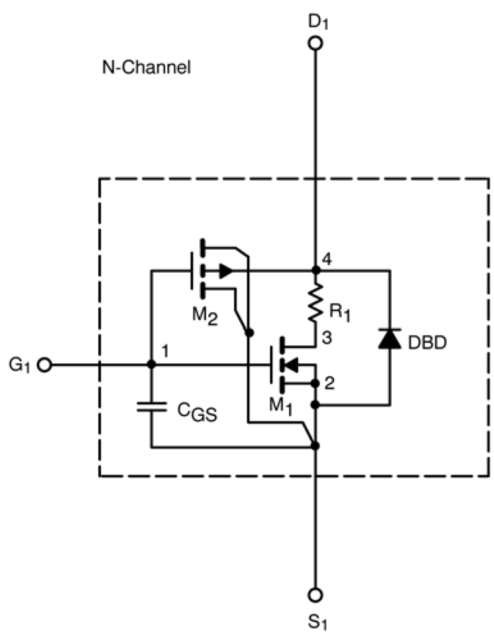
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

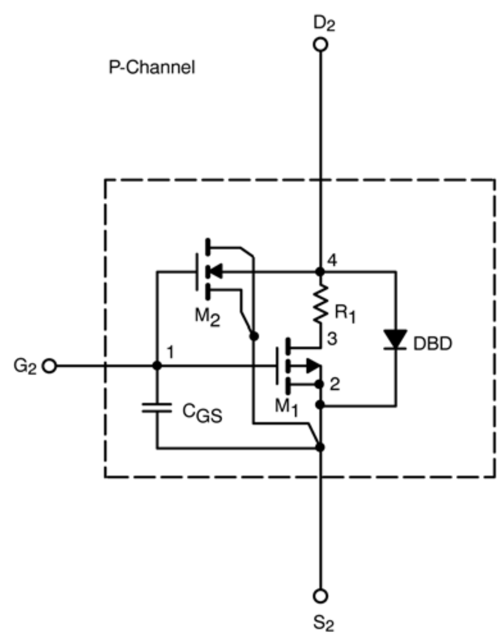
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





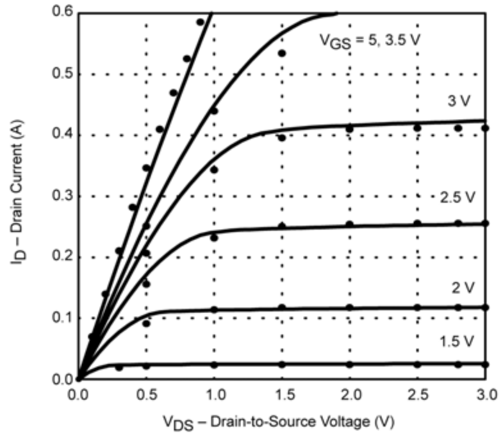
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

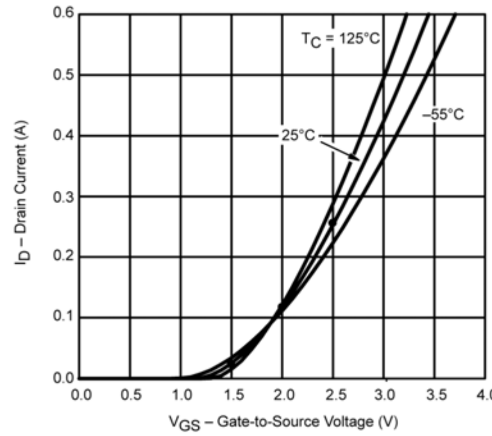
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	1.1		V
		$V_{DS} = V_{GS}$, I_D = –250 µA	P-Ch	1.1		
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 4.5 V	N-Ch	1.1		A
		$V_{DS} \leq -5$ V, V_{GS} = – 4.5 V	P-Ch	3.1		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.29 A	N-Ch	1.64	1.55	Ω
		V_{GS} = –4.5 V, I_D = – 0.41 A	P-Ch	0.85	0.85	
		V_{GS} = 2.7 V, I_D = 0.1 A	N-Ch	2.34	2.8	
		V_{GS} = –2.7 V, I_D = – 0.25 A	P-Ch	1.2	1.23	
		V_{GS} = 2.5 V, I_D = 0.1 A	N-Ch	2.6	3	
		V_{GS} = –2.5 V, I_D = – 0.25 A	P-Ch	1.33	1.4	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 0.29 A	N-Ch	0.33	0.30	S
		V_{DS} = –10 V, I_D = – 0.41 A	P-Ch	0.80	0.80	
Diode Forward Voltage[a]	V_{SD}	I_S = 0.23 A, V_{GS} = 0 V	N-Ch	0.67	0.80	V
		I_S = –0.23 A, V_{GS} = 0 V	P-Ch	–0.76	–0.80	
Dynamic[b]						
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.29 A P-Channel V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –0.41 A	N-Ch	0.55	0.72	nC
			P-Ch	0.52	0.52	
Gate-Source Charge	Q_{gs}		N-Ch	0.22	0.22	
			P-Ch	0.11	0.11	
Gate-Drain Charge	Q_{gd}		N-Ch	0.13	0.13	
			P-Ch	0.14	0.14	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} =10V, R_L = 20 Ω $I_D \cong$ 0.50 A, V_{GEN} = 4.5 V, R_G = 6 Ω P-Channel V_{DD} = –10 V, R_L = 20 Ω $I_D \cong$ –0.50 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch	18	23	ns
			P-Ch	8.8	7.5	
Rise Time	t_r		N-Ch	21	30	
			P-Ch	11	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	21	10	
			P-Ch	11	8.5	
Fall Time	t_f		N-Ch	22	15	
			P-Ch	12	12	
Source-Drain Reverse Recovery Time	t_{rr}	I_S = 0.23 A, di/dt = 100 A/µs	N-Ch	20	20	
		I_S = –0.23 A, di/dt = 100 A/µs	P-Ch	25	25	

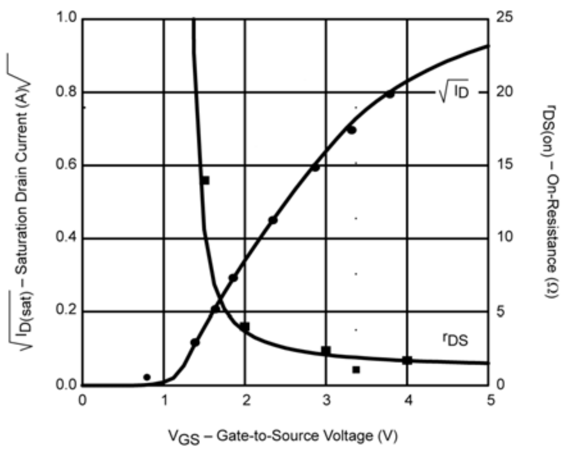
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2.
b. Guaranteed by design, not subject to production testing.

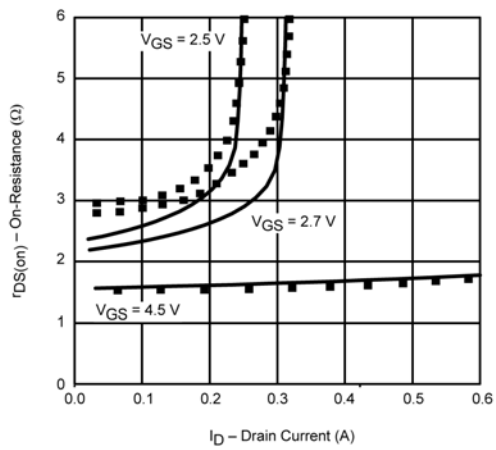
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

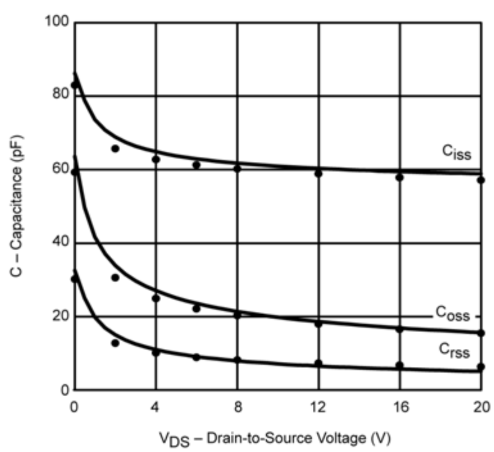
N-Channel MOSFET

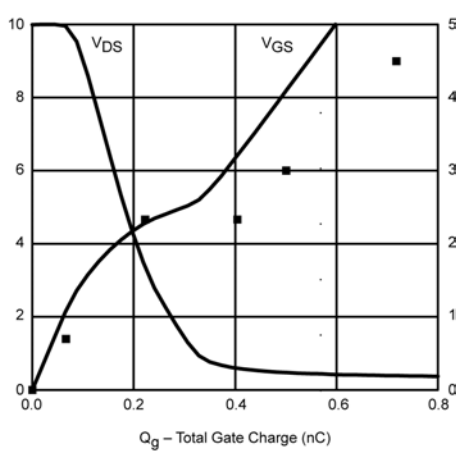






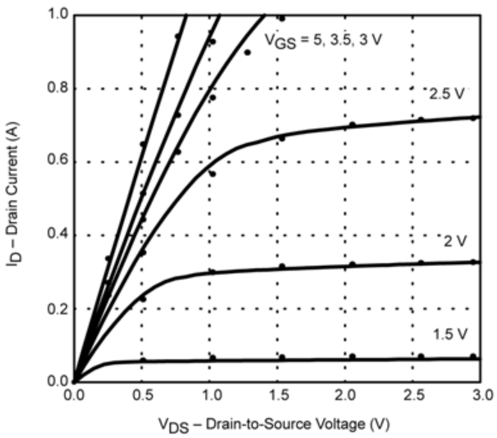


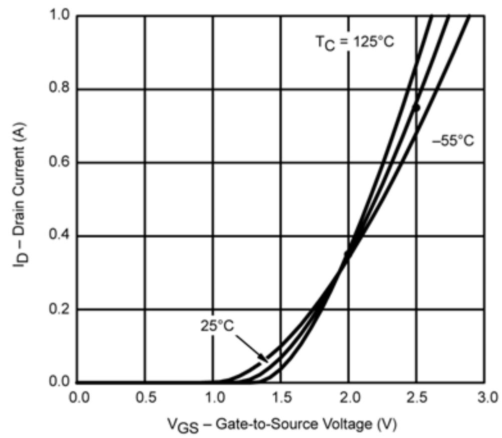


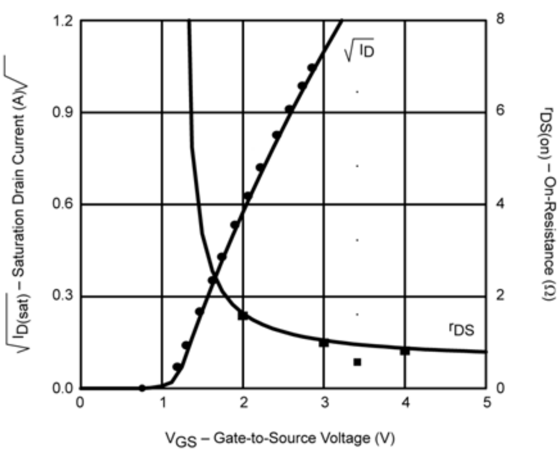


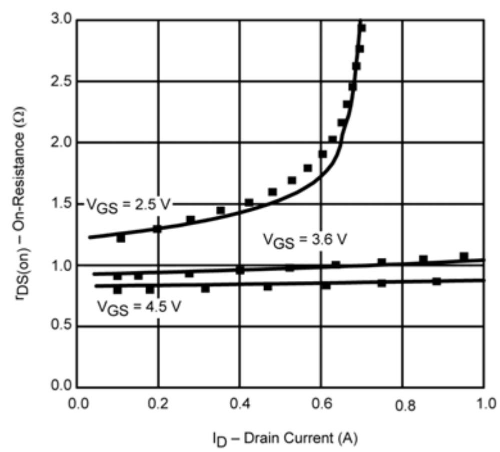
Note: Dots and squares represent measured data.

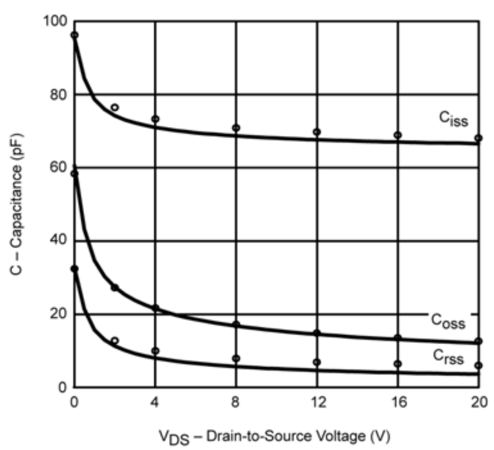
P-Channel MOSFET

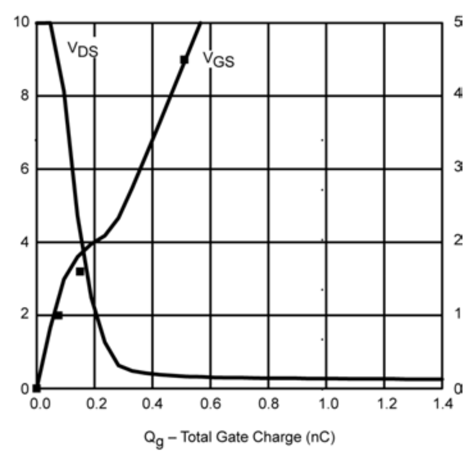












Note: Dots and squares represent measured data.

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